Remarks

Claims 1, 3, 4, 7, 10-18, and 20 are pending in this application. Claims 6, 8, and 19 have been cancelled herein. Claims 1, 7, and 17 have been amended. The Examiner has rejected claims 1, 4, and 6 under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent Publication No. 2003/0046464 to Murty et al. (hereinafter "Murty"). Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Murty in view of U.S. Patent No. 5,809,314 to Carmean et al. (hereinafter "Carmean"). Further, claims 7, 8, 10-15, 17, 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Murty in view of U.S. Patent No. 6,857,084 to Giles (hereinafter "Giles"). Finally, claims 16 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Murty in view of Giles and further in view of Carmean.

A. Claims rejected under 35 U.S.C. 102

Claims 1, 4, and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Murty. Because the Examiner rejected independent claim 1 under section 102(a) on the basis of Murty, each element of the claim must be disclosed in Murty. Murty, however, does not disclose each element of independent claim 1, as amended.

Murty does not disclose that the interrupt handling processor exits from interrupt mode **following the release** of the non-interrupt handling processors from interrupt mode. The Examiner states on page 3 of the Office Action, "During the interrupt-handling mode the first processor will initiate a flag as seen in paragraph 0034 and *handle the interrupt and exit.*" (emphasis added) It is clear that the Examiner states that the first processor, which handles the interrupt, exits after handling the interrupt. Thus, this first processor, the interrupt-handling processor, *does not exit following the release* of the non-interrupt handling processors from interrupt mode. The Examiner later states that the first logical processor acts as an interrupt

handler and releases following the release of the other processors, pointing to page [0049] of Murty. First, Applicant notes that this second assertion by the Examiner is in direct contrast with the Examiner's earlier interpretation of Murty, in which the first processor *exits after handling the interrupt*. Second, the cited portion of Murty, paragraph [0049], at best states that the first logical processor to access a shared register handles the interrupt, executing the interrupt handler. Nowhere does the cited portion of Murty disclose that the interrupt handling processor exits from the interrupt mode **following the release** of the non-interrupt handling processor from interrupt mode, a positively recited claim element of amended claim 1. Thus, for at least these reasons, Murty fails to disclose each and every element of independent claim 1 and, therefore, does not anticipate claim 1. Murty fails to support a finding of anticipation under 35 U.S.C. 102(b). Applicant requests that this rejection be withdrawn. Claims 3 and 4 depend directly or indirectly from independent claim 1 and are therefore allowable for at least the same reason.

B. Claims rejected under 35 U.S.C. 103

Claims 7, 8, 10-15, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murty in view of Giles. Independent claims 7 and 17 each require, in part, that the interrupt-handling processor exits from interrupt mode after each of the non-interrupt handling processors have exited from interrupt mode. As stated above with respect to independent claim 1, Murty fails to teach or suggest this element. The Examiner does not point to Giles to remedy this deficiency. Giles, at best, teaches that processors enter a debug mode as a result of one processor asserting a single debug event signal. (Giles, Abstract). Giles does not teach or suggest all of the required elements of independent claims 7 and 17.

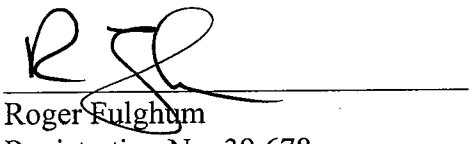
Thus, the combination of Murty and Giles fails to teach or suggest that the interrupt-handling processor exits from interrupt mode after each of the non-interrupt handling

processors have exited from interrupt mode. Because all of the elements of independent claims 7 and 17 are not taught or suggested by the combination of Murty and Giles, a prima facie case of obviousness is not established. In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Here, regardless of whether it is proper to combine the teachings of Murty and Giles, all of the claimed limitations of independent claims 7 and 17 are not shown in the combination. Applicant respectfully submits that the rejection of claims 7 and 17 should be withdrawn and that these claims should be passed to issuance. Claims 8, 10-15, 19 and 20 each depend directly or indirectly from independent claims 7 and 17 and are therefore requested to be passed to issuance for at least the same reasons.

Conclusion

Applicant respectfully submits that claims 1, 3, 4, 7, 10-18, and 20 should be passed to issuance.

Respectfully submitted,



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Date: May 5, 2008